IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

THE TRUSTEES OF PURDUE UNIVERSITY, Plaintiff, v. STMICROELECTRONICS N.V., STMICROELECTRONICS INTERNATIONAL N.V., and STMICROELECTRONICS, INC, Defendants.	CIVIL ACTION NO. 6:21-CV-00727-ADA JURY TRIAL DEMANDED

DECLARATION OF ISHWARA BHAT, PH.D.

I, Ishwara Bhat, hereby declare as follows:

1. I have been retained on behalf of Plaintiff The Trustees of Purdue University ("Purdue") in this case and have been asked to offer an opinion about the disputed terms in U.S. Patent Nos. 7,498,633 (the "'633 Patent") and 8,035,112 (the "'112 Patent") (collectively, the "Asserted Patents").

2. In connection with the preparation of this Declaration, I have reviewed the Asserted Patents, their prosecution history, the parties' respective preliminary claim constructions, the evidence identified in Defendants' disclosure, and Defendants' Opening Claim Construction Brief (Dkt. 66) filed on February 21, 2022, including the attached Declaration of Dr. Vivek Subramanian ("Subramanian Decl.").

3. All of the opinions stated in this Declaration are based on my personal knowledge and professional judgment. If called as a witness, I am prepared to testify competently about them.

4. I am being compensated for work in this matter. My compensation is in no way dependent upon the outcome of this litigation, nor do I have a personal interest in the outcome of this litigation.

5. I reserve the right to supplement, clarify, modify and/or change my testimony as additional facts, questions, or issues come to my attention.

6. This Declaration must not be construed as expressing opinions on matters of law, which are for the Court to determine, although it necessarily reflects an understanding thereof.

I. EXPERIENCE AND QUALIFICATIONS

7. I am a Professor of Electrical, Computer and Systems Engineering Department at Rensselaer Polytechnic Institute (RPI). I joined RPI in 1985 as a research associate and was promoted to full professor in 1999.

8. I received a B.S. degree in Electrical Engineering (B.S.E.E.) from Indian Institute of Technology in 1980, and M.S. and Ph.D. degrees in Electrical Engineering from RPI in 1981 and 1985, respectively.

9. I have over 30 years of experience in the design and fabrication of various semiconductor devices, including in epitaxial growth and characterization of several II-VI, III-V, and IV-IV semiconductors. My work includes growth of wide bandgap semiconductors (such as GaN, SiC, and ZnSe) and narrow band semiconductors (such as HgCdTe and InGaSb). My current research is focused on the processing of silicon-carbide epitaxial films for use in high-power, high-temperature, and high-voltage devices, as well as studying their reliabilities.

10. I have published over 200 refereed journal articles in the area of semiconductor devices and processes, such as wide bandgap semiconductor power devices and their applications. I am also a named inventor on several patents in this field and an associate editor for the Journal of Electronic Materials.

11. I have served as a member of the program committee of several national and international conferences, including serving as co-chair for several U.S. Workshop on the Physics and Chemistry of II-VI Materials, as well as chairing several sessions in international conferences.

12. At RPI, I teach both graduate and undergraduate courses on semiconductor-device physics and device fabrication. The graduate level course deals with both silicon and compound semiconductor materials such as gallium nitride and silicon carbide.

13. A more complete list of my qualifications and experience is set forth in my curriculum vitae, a copy of which is attached hereto as Exhibit A.

II. LEVEL OF ORDINARY SKILL IN THE ART

14. A person of ordinary skill in the art ("POSITA") at the time of invention would have had either an M.S. degree in electrical engineering or related subject with a concentration in the design and fabrication of silicon-carbide power semiconductor devices, or a B.S. degree in electrical engineering or related subject, and two years of experience working with the design and fabrication of silicon-carbide power semiconductor devices. Less work experience may be compensated by a higher level of relevant education, and vice versa, where "relevant" in either case must include design and fabrication of silicon-carbide power semiconductor devices. Based on my education and experience, I meet the qualifications of such person of ordinary skill and know what a POSITA would and would not know.

15. In my opinion, a person with only a semiconductor background but no specific experience in SiC would not be regarded as a POSITA when the art in question is design, fabrication, and operation of SiC devices. For example, and as further explained below, SiC has several unique properties (e.g., a wide bandgap, high breakdown field, and high thermal conductivity) that make SiC especially attractive for high-voltage, high-power, and high-temperature applications and that substantially differentiate it from silicon power devices. *See, e.g.,* 112 Patent at 1:50-53 ("Although silicon has been the material of choice for many semiconductor applications, its ***fundamental electronic structure and characteristics prevent its utilization beyond certain parameters***.") (emphasis added). Given these unique properties, the

design considerations for SiC power devices, and the associated problems addressed during fabrication, are materially different from those governing the design of silicon power devices. Therefore, proficiency in the design and fabrication of silicon power devices does not translate into proficiency in the design of SiC devices.

A. Material Differences Between SiC and Silicon and Their Effect on the Design of Power MOSFETs

16. Generally, the figure of merit (FOM) characterizing the performance of unipolar power devices is $V_B^2/R_{on,sp}$, where V_B is the rated blocking voltage and $R_{on,sp}$ is the resistance × area product (the specific on-resistance). The goal of the power-device designer is to maximize this FOM, i.e., to minimize the on-resistance while maintaining the specified blocking voltage V_B. *See, e.g.*, '633 Patent at 1:18-36; '112 Patent at 1:61-2:6.

17. A power MOSFET has five principal resistance elements in the conductive path: the source resistance, channel resistance, JFET-region resistance, drift-region resistance, and substrate resistance. The goal of the designer is to therefore minimize the sum of these resistance elements, which are remarkably different in SiC and silicon.

18. One of the many differences between SiC and silicon semiconductor physics is that the critical field for avalanche breakdown of the semiconductor is 7 times higher for SiC, compared to silicon. This has two important consequences: (a) **the resistance of a properly designed SiC drift region is approximately 350 times smaller than in silicon at the same blocking voltage**, and (b) the maximum electric field in the oxide under the gates of a SiC device is approximately seven times higher than in silicon at the same blocking voltage.

19. The allowable maximum electric field in the oxide under the gate is about the same for SiC and silicon, in the range of 3–4 MV/cm. This limit is necessary to prevent premature oxide failure after long periods of operation. Since the highest field the semiconductor can support is the

critical field, and the critical field is approximately 7 times higher in SiC than in silicon, the oxide field of SiC MOSFETs can also be approximately 7 times greater than that of silicon MOSFETs. As a result, special care must be exercised to avoid SiC designs in which the oxide field can exceed 3–4 MV/cm. This is not a concern in silicon since the semiconductor will enter avalanche breakdown before the oxide field can exceed 3–4 MV/cm.

20. Due to the differences described in paragraph 19 above, **the gap between p-base regions (the JFET-region width) in a SiC DMOSFET must not exceed a certain maximum width**. In the blocking state, field crowding occurs at the corners of the p-base regions within the cell and at the periphery of the DMOSFET. These effects are usually analyzed by device simulation taking into account the JFET-region width, the JFET-region doping, and the depth of the p-base regions below the surface. These calculations are not necessary to design an operational silicon DMOSFET.

21. When the MOSFET is in the conducting state and the gate voltage is positive, an inversion layer of electrons is induced on the top surface of the p-base regions. This inversion layer creates a conductive path for electrons to flow from the source across the base and into the JFET region, from whence they flow downward through the drift region and substrate into the drain. **The resistance of an inversion layer is approximately 10 times higher in SiC than in silicon** for the same channel length and applied oxide field. At blocking voltages at and below 1200 V (approximately), the channel resistance in a SiC MOSFET is the dominant resistance for the entire device (and is approximately 10 times higher than in a silicon MOSFET). This means that a SiC MOSFET designer will go to great lengths to minimize the channel resistance and will pay much less attention to the drift-region resistance, while a silicon MOSFET designer can ignore the channel resistance and focus on minimizing the drift region resistance (for example, by

incorporating a *superjunction* drift region that increases cost but improves performance). **As such, a SiC MOSFET and a silicon MOSFET have completely different design considerations, owing to the fundamental differences in their respective material properties**.

22. Another physical property highlights the fact that SiC MOSFETs operate very differently from silicon devices. Due to SiC having a hundredfold higher density of trapping states at the oxide/semiconductor interface, the threshold gate voltage required to induce an electron inversion layer *significantly decreases* as the device heats during operation. While this is a negligible effect in silicon devices, a SiC designer must ensure that the room-temperature threshold voltage is sufficiently positive that it cannot go negative when the device heats up. This is because practical power systems require that the device be *normally off*, i.e., that the MOSFET stop conducting if power is lost to the gate circuit. This is not a serious issue in silicon, owing to its much lower temperature coefficient of threshold voltage.

III. LEGAL STANDARDS

23. I have been instructed that the following standards apply to claim construction and indefiniteness.

24. I understand that the words of a claim are to be given the plain and customary meaning that a POSITA would have understood the claim language to have, as of the effective filing date of the patent application, in light of the claims, specification, and prosecution history. A court should derive the meaning of a claim term by looking to the claim language, the specification, and the prosecution history. Claim construction always begins with the language of the claims themselves. A court may also consider evidence extrinsic to the patent, although such evidence is generally less significant than the intrinsic record when determining the meaning of the claim language. I also understand that there is a heavy presumption that a claim term carries its plain and ordinary meaning, and that a court need not construe a term, particularly when the

plain and ordinary meaning of the term is sufficient. Instead, claim construction is necessary only when the meaning or scope of technical terms is unclear.

25. I further understand that a claim is indefinite when, viewed in light of the specification and prosecution history, it does not inform those skilled in the art about the scope of the invention with reasonable certainty. I also understand that a claim is indefinite if only one term or limitation in that claim is indefinite, but that the law does not require complete certainty as to the scope of a claim or term and instead asks that it be precise enough to afford clear notice of what the claim covers. Thus, reasonable, not absolute, certainty is required.

IV. OPINIONS REGARDING DISPUTED CLAIM TERMS OF THE '112 PATENT

A. "a second, thicker oxide layer over said top surface and sidewall of each of said first gate"/ "a gate oxide layer thicker than said substrate surface oxidation layer, over said tops and sides of each of said gates"

26. With respect to this term, Dr. Subramanian states that "the constructions proposed by Purdue are incorrect because, among other reasons, the construction does not require an oxidation layer type of oxide made by a reaction with the material of the gate and, instead, appears intended to include a deposited type of oxide layer, which is contrary to the invention." Subramanian Decl. ¶ 59. I disagree.

27. Purdue's construction, "layer of oxide that is on the tops and sides of each gate and that is thicker than the layer of oxide below each gate," accurately describes the claimed structure based on the claim and the specification, and the fact that it does not in itself specify how that structure is to be created does not make it incorrect. *See, e.g.,* '112 Patent, FIG. 3.

V. OPINIONS REGARDING DISPUTED CLAIM TERMS OF THE '633 PATENT

A. Whether the preamble of Claim 9 is limiting

28. I disagree with Dr. Subramanian's opinions regarding this term because a POSITA would know that Claim 9 of the '633 Patent refers to a DMOSFET in silicon carbide even without

an explicit statement to that effect, and the position of source, base and JFET region, i.e., on the top surface of the silicon carbide would be apparent in light of the claim language, the specification and the drawings.

29. The ’633 Patent describes high-voltage power semiconductor devices and the descriptions prior to Claim 9 further relate to metal-oxide semiconductor field-effect transistors (MOSFETs) in silicon-carbide. *See, e.g.*, ’633 Patent, Abstract (“A semiconductor device, such as a metal-oxide semiconductor field-effect transistor, includes a semiconductor substrate, a drift layer formed on the substrate, a first and a second source region, and a JFET region defined between the first and the second source regions.”); 1:40-67; FIG. 1.

30. The body of Claim 9 recites defining base-contact regions in a given source region over a drift layer and silicon-carbide substrate. As described in the ’633 Patent specification and drawings, base-contact regions and source regions have different doping. *Id.* FIG. 1; 6:63-7:12. In SiC semiconductors, each doping is achieved by implantation (rather than the diffusion technique available in silicon semiconductors). The “D” in DMOSFET stands for double implantation since the base and the source regions are fabricated by two implantations. Thus, a POSITA would understand that Claim 9 relates to a double-implanted MOSFET based on the claim limitations “a plurality of first base contact regions defined in the first source region” and “a plurality of second base contact regions defined in the second source region.” ’633 Patent, Claim 9.

B. “less than about three micrometers”

31. In my opinion, as explained below, the phrase “less than about three micrometers,” as used in the ’633 Patent and in Claim 9, means exactly that. Further, a POSITA would reasonably understand that “about,” when referring to numerical values such as in the ’633 Patent generally implies ±10% variation. Thus, a POSITA would readily understand the scope of this term with reasonable certainty.

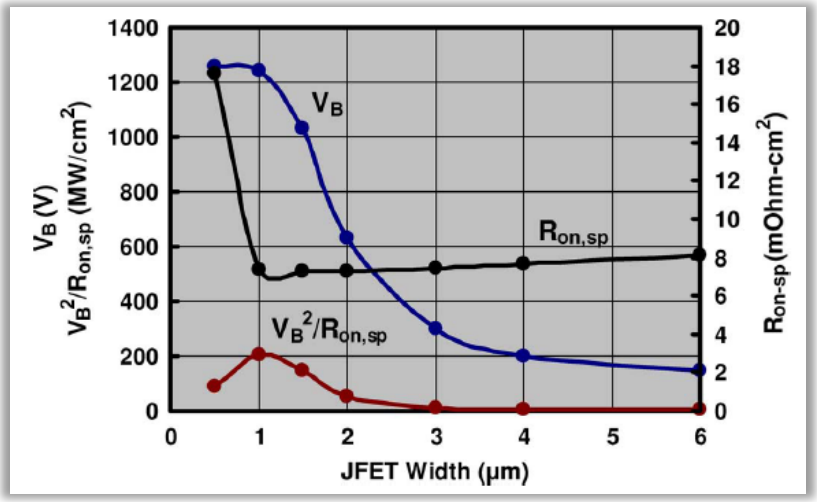
32. Dr. Subramanian's opinions regarding this term are incorrect because, among other reasons, the fabrication of SiC semiconductor devices is a manufacturing process that necessarily produces some uncertainty in the measurement of precise values in the manufactured devices. This means that while, on average, the measurement of a device will be close to the specified value, any two devices fabricated using the fabrication process will have some deviation from this average. For example, the JFET region in the DMOSFET is fabricated by the ion-implantation process using a mask that defines the p-type base region. During the design phase, the p-well mask specifies the JFET width, which can be done precisely. However, upon fabrication, the width of the manufactured JFET depends on several factors, one being the transverse (or lateral) straggle of the ion-implantation species. Transverse straggle measures the distribution of the implanted species along the transverse direction and is dependent on many factors such as the implanting species, the host material, the implantation energy, and the final annealing temperature. Because the ion implantation process results in a distribution of the species in the vertical direction with a mean value called vertical range (R_P), and a distribution of species along the lateral direction called transverse straggle ($R_\perp$), a POSITA would know that the JFET width after fabrication cannot be specified to exact values, but rather a distribution with range and standard deviation.

33. Another important variation in the manufacturing process is the critical dimension variation ("CD variation") of the implant mask that defines the gap between adjacent p-base regions (i.e., the JFET width) due to variations in the photoresist exposure and develop processes, and variations in the subsequent etching of the hard mask that defines the p-base implant gap (i.e., the JFET width). The CD Variation is typically on the order of ±0.2 micrometers, adding to the uncertainty in reproducing an exact width in practice.

34. As mentioned in paragraph 15 above, a POSITA would understand that the goal of

the device design is to achieve the lowest possible on-resistance while still meeting the desired blocking voltage specification. Although this introduces some design tradeoffs, these are by no means subjective as Dr. Subramanian suggests. A POSITA would understand that a JFET region that was too wide would result in the field across the oxide under the gate in the blocking state to exceed a maximum field of 3–4 MV/cm needed for good long-term oxide reliability. On the other hand, a JFET region that was too narrow would increase the on-state resistance, which is against the design goal of the lowest possible on-resistance. Therefore, there is an optimum width at which one achieves the lowest on-resistance without allowing the oxide field to exceed the electric field for oxide breakdown in the blocking state.

35. The purpose of restricting the JFET-region width is to minimize the area of the unit cell, thereby increasing the cell density and reducing the on-state resistance. A POSITA would understand that the goal of the design is to increase the density by decreasing the size of individual MOSFET cell pitch, and achieving this by using the lowest JFET-region width with the stated constraints above. A POSITA would know the design criteria of JFET-region width generally and from published literature. For example, in a 2007 paper by the inventors of the ’633 Patent, which is referenced in the ’112 Patent, the JFET-region design was attempted from 0.5 to 6 micrometers, and based on Figure 2, shown below, it is clear to any POSITA that there is no improvement in the figure of merit for a MOSFET beyond a JFET-region width of about three micrometers. Saha and Cooper, IEEE Transactions on Electron Devices, Vol. 54, 2007, p2786, attached hereto as Exhibit B.



36. So, a POSITA would not extend the JFET all the way to 10 micrometers because there would be no performance benefit and increasing the size of the MOSFET would decrease the cell density. *See also* Sei-Hyung Ryu, Anant K. Agarwal, Nelson S. Saks, Mrinal K. Das, Lori A. Lipkin, Ranbir Singh & John W. Palmour, "Design and Process Issues for Silicon Carbide Power DiMOSFETS," in Mat. Res. Soc. Symp. Vol. 640, pp. H4.5.1 – H.4.5.6 (2001) (evaluating 2-5 micrometer JFET width and concluding three micrometers is optimal), which is attached hereto as Exhibit C. A POSITA would also understand that the JFET width of "less than about three micrometers" does not mean zero micrometers since at zero there is no DMOSFET present. The lower bound for JFET width is limited by the manufacturing process technology. The '633 Patent gives an example of "about one micrometer." '633 Patent at 1:65-67; 2:47-49; 3:25-26; *see also* Claim 10.

37. A POSITA would also know that "a typical DMOSFET device" as used in the '633 Patent does not mean a logic MOSFET but rather a SiC power MOSFET. The '633 Patent relates to high-voltage semiconductor devices, as is evident from the title, and the specification further refers to power MOSFETs and not logic MOSFETs. Most logic MOSFETs are low voltage devices and SiC materials are sought for high voltage power devices because of its significant advantages

over silicon, some of which are discussed above. A POSITA would understand that a DMOSFET would never be used as a logic MOSFET.

38. Based on this, it is my opinion that "less than about three micrometers," as used in the context of the '633 Patent, is not indefinite because a POSITA would readily understand the scope of the term with reasonable certainty.

03/14/2022

Date

Ishwara Bhat, Ph.D.